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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,611	11/18/2003	Tzu-Ching Tsai	10113171	4874

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QUINTERO LAW OFFICE
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EXAMINER	
PHAM, THANHHA S	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,611	TSAI ET AL.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20* is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Applicant's Amendment After Non-Final Rejection dated 06/08/2005.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al. [US 6,069,038] in view of Uhlenbrock et al. [US 6,271,131].**

► With respect to claims 1, 4 and 11, Hashimoto et al. (figs.3-19, cols. 9-13) discloses a method of a filling bit line contact via, comprising:

providing a substrate (1, fig. 7) having a device region (memory cell region including gate electrode 8A) and periphery region (logic LSI including gate electrode 8B), the device region having a transistor with a gate electrode (8A), drain region (11), and source region (11) on the substrate (1);

forming a dielectric layer (22) overlying the substrate, the dielectric layer having a bit line contact via (24) exposing the drain region (11, fig. 13, col. 11 lines 38-46), and

periphery contact via (33, fig. 17, col. 12 lines 23-32) exposing the periphery region (fig. 17, col. 12 lines 23-32);

forming a doped conductive layer (26, fig.14) overlying the drain region (11), dielectric layer (22), and periphery region (col. 12, lines 1-7: doped polysilicon being formed on nitride 22);

removing the doped conductive layer (26) using etching, thereby remaining the doped conductive layer (26), lower than the dielectric layer (22), overlying the drain region (11) (fig. 16, col. 12 lines 20-23);

conformally forming a barrier layer (titanium nitride film) overlying the dielectric layer (22), doped conductive layer (26), and periphery region (fig. 18, col. 12 lines 58-67 and col. 13 lines 1-2); and

forming a first conductive layer (tungsten film) filling the bit line contact via and periphery contact via (fig. 18, col. 12 lines 58-67 and col. 13 lines 1-2).

Hashimoto et al. substantially discloses all the limitation as claimed above except etching the doped conductive layer (26) lower than the top surface of the gate electrode.

However, Uhlenbrock et al. (figs. 4-6, col. 7 lines 16-31) discloses etching the doped conductive layer (150) lower than the top surface of the gate electrode (124, 126). Therefore, at the time the invention was made, it would have been obvious to one ordinary skill in the art to etch the doped conductive layer lower than the top surface of the gate electrode as taught by Uhlenbrock et al. into the process of Hashimoto et al. in order to form the conformal barrier layer which protects the subsequently deposited

capacitor dielectric against diffusion from underlying plug and other surrounding material (col. 7, lines 26-31).

► With respect to claims 2 and 12, Hashimoto et al. (fig. 11, col. 11 lines 34-37) discloses that the dielectric layer (22) is an oxide layer.

► With respect to claims 3 and 13, Hashimoto et al. (fig. 14, col. 12 lines 24) discloses that the doped conductive layer (26) is polycrystalline silicon doped with As.

► With respect to claims 5, 6, 14 and 15, Hashimoto et al. (fig. 18, col. 12 lines 58-64) discloses that the barrier layer (TiN) prevents the diffusion of the first conductive layer.

► With respect to claims 7 and 16, Hashimoto et al. (fig. 18, col. 12 lines 60-61) discloses that the first conductive layer is tungsten.

► With respect to claims 8 and 17, Hashimoto et al. (fig. 8, col. 10 lines 47-50) discloses that the periphery region is a doped region (16).

► With respect to claims 9 and 18, Hashimoto et al. (fig. 6, col. 9 lines 34-51) discloses that the periphery region is a second conductive layer (8B), and the gate electrode (8B) further comprises the second conductive layer (8B).

► With respect to claims 10 and 19, Hashimoto et al. (fig. 6, col. 9, lines 31-51) discloses that the second conductive layer (8B) is a silicide layer comprising tungsten.

2. **Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al. [US 6,069,038] in view of Rhodes [US 6,458,651]**.

► With respect to claims 1, 4 and 11, Hashimoto et al. (figs.3-19, cols. 9-13) discloses a method of a filling bit line contact via, comprising:

providing a substrate (1, fig. 7) having a device region (memory cell region including gate electrode 8A) and periphery region (logic LSI including gate electrode 8B), the device region having a transistor with a gate electrode (8A), drain region (11), and source region (11) on the substrate (1);

forming a dielectric layer (22) overlying the substrate, the dielectric layer having a bit line contact via (24) exposing the drain region (11, fig. 13, col. 11 lines 38-46), and periphery contact via (33, fig. 17, col. 12 lines 23-32) exposing the periphery region (fig. 17, col. 12 lines 23-32);

forming a doped conductive layer (26, fig.14) overlying the drain region (11), dielectric layer (22), and periphery region (col. 12, lines 1-7: doped polysilicon being formed on nitride 22);

removing the doped conductive layer (26) using etching, thereby remaining the doped conductive layer (26), lower than the dielectric layer (22), overlying the drain region (11) (fig. 16, col. 12 lines 20-23);

conformally forming a barrier layer (titanium nitride film) overlying the dielectric layer (22), doped conductive layer (26), and periphery region (fig. 18, col. 12 lines 58-67 and col. 13 lines 1-2); and

forming a first conductive layer (tungsten film) filling the bit line contact via and periphery contact via (fig. 18, col. 12 lines 58-67 and col. 13 lines 1-2).

Hashimoto et al. substantially discloses all the limitation as claimed above except the doped conductive layer (26) lower than the top surface of the gate electrode.

However, Rhodes (fig. 2, col. 3 lines 60-67) discloses that it is known in the art to form the doped conductive layer (34) lower or above the top surface of the gate electrode (17,18). Therefore, at the time the invention was made, it would have been obvious to one ordinary skill in the art to form the doped conductive layer lower than the top surface of the gate electrode as taught by Rhodes into the process of Hashimoto et al. in order to form the conformal barrier layer which protects oxygen diffusion from doped conductive layer and other surrounding material.

► With respect to claims 2 and 12, Hashimoto et al. (fig. 11, col. 11 lines 34-37) discloses that the dielectric layer (22) is an oxide layer.

► With respect to claims 3 and 13, Hashimoto et al. (fig. 14, col. 12 lines 24) discloses that the doped conductive layer (26) is polycrystalline silicon doped with As.

► With respect to claims 5, 6, 14 and 15, Hashimoto et al. (fig. 18, col. 12 lines 58-64) discloses that the barrier layer (TiN) prevents the diffusion of the first conductive layer.

► With respect to claims 7 and 16, Hashimoto et al. (fig. 18, col. 12 lines 60-61) discloses that the first conductive layer is tungsten.

► With respect to claims 8 and 17, Hashimoto et al. (fig. 8, col. 10 lines 47-50) discloses that the periphery region is a doped region (16).

► With respect to claims 9 and 18, Hashimoto et al. (fig. 6, col. 9 lines 34-51) discloses that the periphery region is a second conductive layer (8B), and the gate electrode (8B) further comprises the second conductive layer (8B).

► With respect to claims 10 and 19, Hashimoto et al. (fig. 6, col. 9, lines 31-51) discloses that the second conductive layer (8B) is a silicide layer comprising tungsten.

Allowable Subject Matter

3. Claim 20 is allowed.

4. The following is a statement of reasons for the indication of allowable subject matter: Recorded Prior Art fails to disclose or suggest the combination of the process steps of filling a bit line contact via as recited in the base claim 20 including conformally forming a doped conductive layer overlying the drain region, dielectric layer, and periphery region.

Response to Arguments

5. Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thanhha Pham

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